|| न हि ज्ञानेन सदृशं पवित्रमिह विद्यते ||
Dr. Vitthalrao Vikhe Patil Foundation's
Dr. Vithalrao Vikhe Patil
College of Engineering Ahmednagar
DTE College Code: EN-5161

Date: 02/10/2023

Notice

All the S.E, T.E, B.E. students are hereby informed that Training &Placement cell of Electronics and Telecommunication Engineering Department is arranging Webinar (Online Mode) on "Job opportunities in VLSI/ Semiconductor Domain "conducted by Takshila VLSI Technology, Bangaloreon Friday 4 /10/202 at 06:30 pm.

All the students should present for Webinar

This is for strict compliance.

Prof. A.R. Landge
T&P cellIn charge

Dr. Anita K. Patil
H O D

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Dr. Vithalrao Vikhe Patil Foundation's
Dr. Vithalrao Vikhe Patil College of Engineering
Affiliated to SPPU, Pune (ID. No. PU/AN/Engg./027/(1983)
Recognized by AICTE, New Delhi & Government of Maharashtra
Accredited by NAAC with A+ Grade (3.34 CGPA) & NBA, New Delhi
Estd. 1983
Dr. Vithalrao Vikhe Patil Foundation
Ahmednagar

Ref.No. CEA/E&TC/2023/2812

Date:-29/09/2023

To,

Mr. Manoj,

Physical Design Engineer,

Takshila VLSI Technology,

Bangalore,.

Subject: Request for conducting Expert lecture "**Job opportunities in VLSI/ Semiconductor Domain**"on 04thOctober 2023.

Dear Sir,

It gives us immense pleasure to state that the Training & Placement cell of Department of Electronics & Telecommunication Engineeringof our institute organizes a webinar for students.

As per discussion with Prof. A.R.Landge, Assistant Professor, Department of Electronics & Telecommunication Engineering,We would like to invite you to conducta Webinaron topic "job opportunities in VLSI /Semiconductor Domain"on 04th October 2023 .

Kindly accept our invitation to deliver lecture and give your consent.

Thanking you.

Yours sincerely,

(Dr. Uday P. Naik)

Principal

Principal
College of Engineering
Ahmednagar

NAAC A+

DR. VITHALRAO VIKHE PATIL COLLEGE OF ENGINEERING, AHMEDNAGAR

www.enggnagar.com principal@enggnagar.com 0241-2777296 / 2779496 / 9356164515
Vilad Ghat, Vadgaon Gupta, PO MIDC, Ahmednagar(MS) India - 414 111

Report of Webinar

Topic	Job opportunities in VLSI/ Semiconductor Domain
Date:	4th October 2023
Speaker	Mr. Manoj, Physical Design Engineer, Takshila VLSI Technology, Bangalore
Industry:	Takshila VLSI Technology
Time	6.30 p.m – 8.00 p.m
No. of Participants	134
Venue	E&TC Department
Event In charge	Prof. A.R. Landge

Prof. A.R. Landge
Event In charge

Dr. Anita K. Patil
H O D

Course Outcomes

Co1: Students will get the knowledge about essential skills required for working in VLSI industry

Co2: Student will be able to learn in practical aspects of VLSI design

CO-PO Mapping

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	P012
CO1									2	2	2	
CO2									2	2		

CO-PSO Mapping

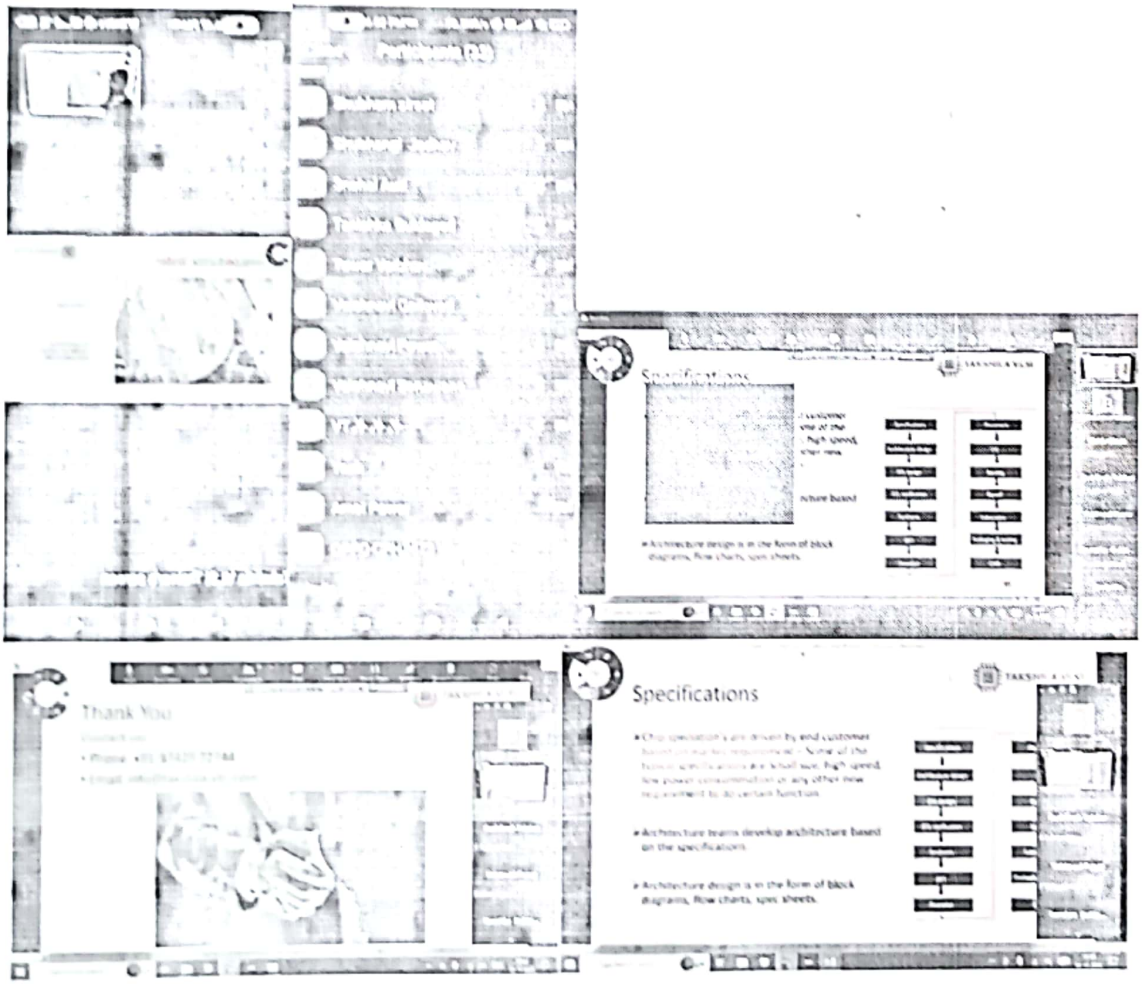
CO	PSO1	PSO2	PSO3
CO1			1
CO2		1	

Job opportunities in VLSI/ Semiconductor Domain

Contents:

- Basics of CMOS
- MOSFET Operation, stick diagram, IC fabrication process
- Basic understanding of transition/slew, capacitance, leakage power, internal power, On-Chip-Variation (derate, AOCV, LVF)
- Library file difference NLDM, CCS, ECSM, LVF
- Timing concepts understanding like setup, hold, recovery, removal, pulse_width, clock gating check
- PLL jitter understanding and uncertainty calculations
- IO budgetting
- Different Timing Modes understanding
- ECO generation
- Floorplaning concepts and IO placement
- Power planning
- Placement strategies like region, fence, blockages, pading, bump, dont touch, filler gap
- DRV optimization, Buffer tree synthesis
- Clock tree synthesis and clock latency calculations
- Routing design and optimization
- Antenna
- ECO Timing closure and implementation cycle
- Design Rule Checks understanding and importance
- Layout Versus Schematic and difference with respect to LEC
- Electrical Rule Checks
- IR Drop analysis - Static and Dynamic

Photographs :



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Dr. Vitthalrao Vikhe Patil Foundation's

Dr. Vithalrao Vikhe Patil College of Engineering Ahmednagar

DTE College Code: EPI 5161

Feedback Form

Date: 04/10/2023

Topic of Expert Lecture: Webinar on "**Job opportunities in VLSI/ Semiconductor Domain**

"

Name of Expert: **Mr. Manoj, Physical Design Engineer, Takshila VLSI Technology, Bangalore**

Q.1 How would you rate the topic of Webinar?

Average ☐ Good ☐ Excellent ☐ Outstanding ☑

Q.2 How was the level of content?

Average ☐ Good ☐ Excellent ☑ Outstanding ☐

Q.3 How would you rate the knowledge of Resource person?

Average ☐ Good ☐ Excellent ☐ Outstanding ☑

Q.4 How did you like the subject material?

Average ☐ Good ☐ Excellent ☑ Outstanding ☐

Q.5 Will lecture be useful for your studies?

Average ☐ Good ☐ Excellent ☑ Outstanding ☐

Q.6 How did you rate the lecture overall?

Average ☐ Good ☐ Excellent ☐ Outstanding ☑

Q.7 Remark

more such events should be encouraged

Q.8 Suggestions if any?

frequency of events should be more

Boards should

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Ahmednagar

Ref.No. CEA/E&TC/2023/ 290 | Date:-05/10/2023

LETTER OF THANKS

Dear Sir,

On behalf of Dr. Vithalrao Vikhe Patil College of Engineering, Ahmednagar, we take this opportunity to extend our heartfelt gratitude & huge **"Thank you"** for delivering webinar on**"Personality Development and getting job ready"**for Electronics & Telecommunication Engineering students on 04/10/2023 at 6:30 pm.

Let us maintain and cherish these relations for mutual benefit hence and forever.

We shall remain obliged for sparing valuable time with us.

(Dr. Ms.A.K.Patil)
HOD, E&TC

(Dr. Uday P. Naik)
Principal
Principal
College of Engineering
Ahmednagar

To,
Mr. Manoj,
Physical Design Engineer,
Takshila VLSI Technology ,
Bangalore,